WHY CLEAN A NO-CLEAN FLUX

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ABSTRACT
Residues present on circuit boards can cause leakage currents if not controlled and monitored. How "Clean is Clean" is neither easy nor cheap to determine. Most OEMs use analytical methods to assess the risk of harmful residues. The levels that can be associated with clean or dirty are typically determined based on the exposed environment where the part will be deployed. What is acceptably clean for one segment of the industry may be unacceptable for more demanding segments.

As circuit assemblies increase in density, understanding cleanliness data becomes more challenging. The risk of premature failure or improper function is typically site specific. The problem is that most do not know how to measure or define cleanliness nor can they recognize process problems related to residues. A new site specific method has been designed to run performance qualifications on boards built with specific soldering materials, reflow settings and cleaning methods. High impedance measurements are performed on break off coupons designed with components geometries used to build the assembly. The test method provides a gauge of potential contamination sources coming from the assembly process that can contribute to electrochemical migration.

THE AGE OF NO CLEAN SOLDERING MATERIALS
The Montreal Protocol, a treaty designed to protect the ozone layer, was enacted September 16, 1987.[1] The treaty restricted, and in some cases, banned numerous substances that contribute to ozone depletion. At this time in history, many assemblers used rosin based flux compositions as an aid to enable soldering of components onto a circuit assembly. Solvent based cleaning agents, most notable CFC-113, were used to clean the rosin fluxes off the assembly post soldering.

Highly reliable circuit assemblies were built around standards developed and tested by the United States Military. All assemblies built for long life and failure prevention were cleaned. Solvent based cleaning agents matched up to rosin based flux compositions, and as such, were the dominate cleaning technology used to clean printed circuit boards. Solvent based cleaning is a highly efficient method of cleaning by using a low boiling solvent composition to wash, rinse and dry the assembly.

Many of the solvents used to clean printed circuit boards were classified as ozone depleting substances. Once the Montreal Protocol was ratified, industry sought out alternatives to ozone depleting substances. One of those alternative was No-Clean soldering materials.

At that time, through hole, leaded components and connectors were dominate technologies. Semiconductor packages were just emerging. The spacing between many conductors was 25 mils or greater at this time. With few to no drop-in cleaning solvents that were a direct substitute for ozone depleting cleaning solvents, the soldering material companies introduced a disruptive innovation called "No-Clean" solder fluxes and pastes designed for through hole and surface mount soldering.

The no-clean soldering materials used a combination of solvents, activators and rheological additives that left a low non-ionic residue. The activators within the flux were designed to be heat activated. With proper heat exposure, these activators would oxidize and reduce into a benign residue that was encapsulated into a resin/rosin residue. The keys to implementing 'No-Clean" technology required cleanliness specifications on incoming boards and components, clean manufacturing sites, material handling protocols and packaging techniques designed to prevent the transference of problematic ionic residues.

BUILDING TO A NO-CLEAN STANDARD
As circuit densities increase (smaller lines and spaces), the electrical bias across the smaller space results in a higher voltage gradient between conductors. For an assembler who utilizes some form of cleaning, the increased circuit density often means a greater challenge to complete cleaning. For an assembler who does not utilize an assembly cleaning process, the cleanliness of incoming components and boards becomes critical as there is no opportunity to remove harmful residues in the printed board assembly process.

A wide range of contamination sources must be considered when building to a No-Clean standard. Sources of contamination comprise the following:

- Component fabrication residues
- Printed Circuit Board plating and solder mask residues
- Flux residues
- Material handling induced from human body fluids, oils and organic residues
- Processing equipment
- Unique/Non-Standard processes and materials
- Touch-up, Repair and testing operations

Residues on printed circuit boards and components are directly related to the reliability of the final product. Two primary questions are

1. How is cleanliness measured and controlled?
2. How clean does incoming parts need to be?

At the time of the Montreal Protocol, a pass / fail test method titled "Resistivity of Solvent Extract" (R.O.S.E.) was used. The test method used an extraction solvent composition of 75% Isopropyl alcohol / 25% DI water, which readily dissolved rosin residues and provided a bulk level of ions present on the circuit board. R.O.S.E. test methodology was adopted by printed circuit board and component manufacturers to measure incoming part cleanliness.

As components, soldering materials and assemblies decreased in size, the ability to rely on the R.O.S.E. methodology became less reliable. The determination of "How Clean is Clean" enough was neither easy nor cheap to determine. The following factors drove the decision:

- The end use environment
- The design/service life
- The technology used (high frequency, high voltage etc.)
- The consequences of failure

OEMs developed correlation test methods comprising:

- Accelerated Life Testing
- Heat / Vibration
- Temperature / Humidity
- Thermal cycling

Properly studied, these test methods detected residues that are harmful/benign and the levels that can be associated with clean or dirty.

As printed circuit assemblies become more dense and populated with leadless components, there is an increased risk of premature failure or improper function due to residues present under component terminations. Standard test protocol and industry standards may no longer be applicable. As such, there is a greater challenge to correlating cleanliness related data electrical functions and failures. With these complications, OEMs must determine the following:

- Data to generate
- How much data to generate?
- The meaning or context of the data
- What to do with the data?

The answers to these complications depend on the test method, the company and customers involved.

CORROSION FORMATION ON PCBs

Corrosion accounts for more than 50% of electrical system failures.[2] Harsh environments can cause electrochemical migration, unintended power disruption and intermediate connection. Designing for Reliability requires

- Material specifications
- Modeling corrosion risks
- Component selection
- Corrosion prevention

When the finished product is exposed to harsh environments, low electrical resistance between conductors must be understood (Figure 1).

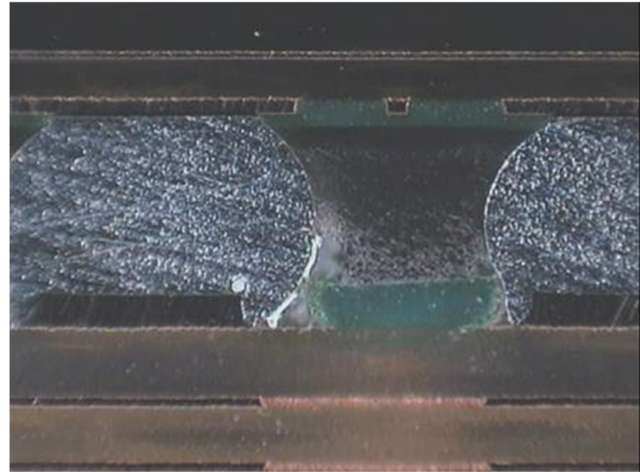

Figure 1: Inter-Conductive Spacing

Chemicals in synergistic combination with heat and moisture promote metallic corrosion. Electrical fields are induced by magnetic forces of attraction (Figure 2).

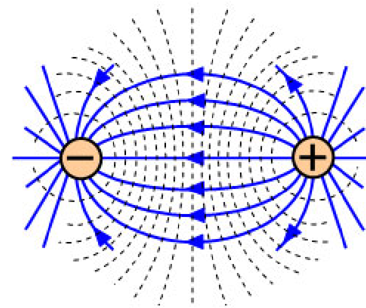

Figure 2: Electric Field Attractive Forces[3]

Metallic surfaces differ from all other materials. Atoms in the outer shell of metals are loosely bound. When an applied force is applied, these loosely bound electrons travel in the direction of the force, forming an electric current.

In contrast to metals, water is an exceptional solvent due to its electro-negative / positive structure. Water likes to keep electrons to itself.

- Partial negative charge at the oxygen end
- Partial positive charge at the hydrogen end

The partial negative is attracted to the partial positive. Ions readily dissolve in water. An anion wants to give an electron while a cation wants to donate an electron. This bonding effect makes water a perfect electrolytic solution. Problematic ions dissolved in water remove metal oxides. These oxides migrate in the present of a strong electrical field.

When the electrolytic solution comes in contact with the solder alloy, component metallization and pad, metal oxides

can dissociate into the electrolyte. The metals mobilized in the electrolyte can plate out in the form dendrites.[4] The leakage currents from these dendrites reduces resistivity. Ionic residues are mobilized based on the strength of the ion-dipole forces of attraction with water. The intermolecular bond resistivity.

Corrosion occurs when a metal is mobilized within the water electrolytic solution. Water reduces the metal ion forming an aqua-metallic solution along at a pH value dependent on the ion dissolved. Conduction happens when these ions travel within an electric field (Figure 3).[5]

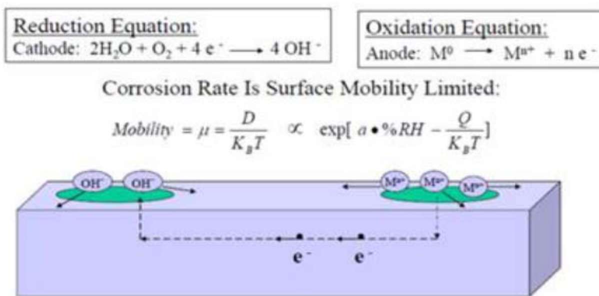

Figure 3: Corrosion Rate is Surface Mobility Related

At 60% relative humidity, three monolayers of moisture can form on the surface. This is all it takes to mobilize problematic ions.

ELECTROCHEMICAL MIGRATION

Electrochemical migration is the growth of conductive metallic filaments through an electrolytic solution under a DC voltage bias.[6] The failures can be intermediate or permanent. Leakage currents depend on the current density and formation of the resulting dendrites. Miniaturization increases device sensitivity, surface contamination and flux residues. Device failure is strongly affected by the chemistry of assembly materials. Key factors are the activity and ionic nature of residues. Metal migration is dependent on PCB material composition, board surface roughness, concentration and distribution of residues and environmental conditions. Key factors are

- Inter-conductor spacing
- Voltage bias
- Active residue
- Temperature
- Humidity

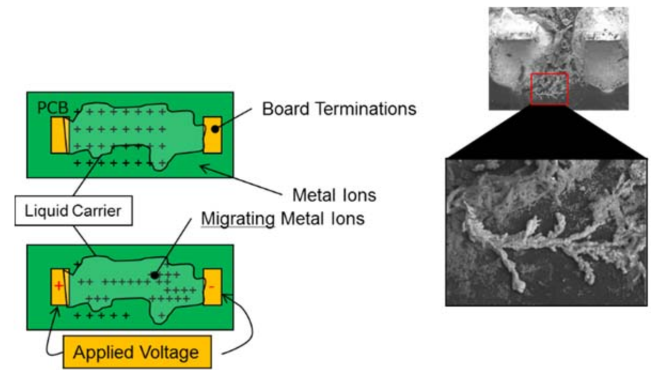

Figure 4: Electrochemical Path Formation

TEST METHOD ADVANCEMENTS

Electrochemical failures are typically site specific. Bottom terminated components have a near chip-scale structure, very good electrical performance, low profile and good thermal dissipation. The low profile creates key factors that can affect part reliability.

- Channel for flux to outgas during reflow is blocked
- Active flux accumulates under component terminations
- Difficult cleaning challenge
- Electric field is increased due to the small interconductor spacing

Industry accepted test methods used to determine cleanliness are Ion Chromatography (IC) and Surface Insulation Resistance (SIR). A key limitation of both methods is the ability to isolate and determine the activity of the flux residues trapped under component terminations.

IC analysis quantifies ions present on the circuit assembly. The levels are reported as an average of the board and component surface area. Problematic contamination is typically located under leadless components. Under these components, the ion levels can be highly concentrated. When averaging the IC results over the total surface of the board, the problematic levels under site specific components can be averaged down, with levels within a safe threshold. One IC method designed to address this limitation is the C3 Site Specific method. Even with this method, isolation and quantification of problematic ions is still challenging.

The IPC-B-52 test board allows for site specific measurements for each component inserted. The open and pattered SIR data points place the trace at the pad termination. The SIR data points are not targeted under component terminations where active flux residue is trapped.

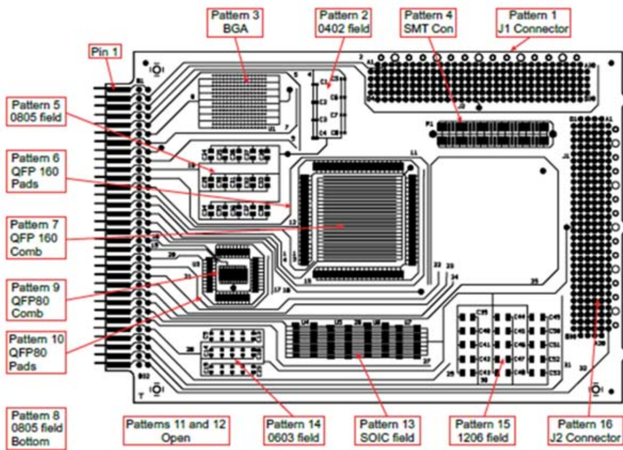

Figure 5: IPC-B-52 Test Board Design

SIR test board advancements have been designed with the SIR data point's taken in the spacing under the component termination (Figure 6). The test board objective is to evaluate the flux activity and its potential to mobilize in the presence of moisture and bias. The SIR sensors provides insight into the activity of residues where electrochemical migration takes place.

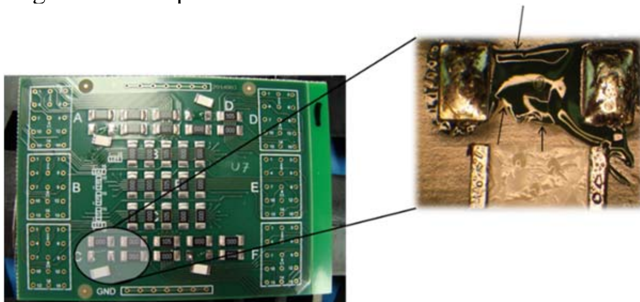

Figure 6: Sensors Place in Area Separating Conductors

The SIR test board and method is designed to test resistance drop due to contamination, voltage bias, humidity and temperature effects; flux residue activity and conductor pitch. Pockets of contamination are influenced by the cleanliness of incoming parts, component type, density (placement), solder paste volume, flux type, reflow conditions, activation temperature and standoff height. Conductivity and hydroscopic nature of the residue under the component termination is site in which failure initiates.

The test boards can be designed to study options for increasing standoff height. Past research finds that flush mounted components entrap flux residue. Elevating the standoff provides a channel for flux to outgas. Flux outgassing channels minimize the flux residue under the component, reduces the activators levels within the flux to a benign state, hardens the residue, and reduces the potential of the residue to be mobilized in the presence of humidity. With these factors being a reliability concern, the sensor test board can be used to develop a risk profile. The board can also be used to evaluate solder paste and cleaning options.

One test board design studies design options for quad flat pack no lead (QFN) components. The design provides insight into solder mask definition strategies, vias within the ground lug, solder mask with vias within the ground lug and standoff methodologies (Figure 7). These design options allow the OEM to run designed experiments to study solder paste flux residues, reflow parameters and cleaning options. The data sets provide insight into each of these factors for optimizing process conditions.

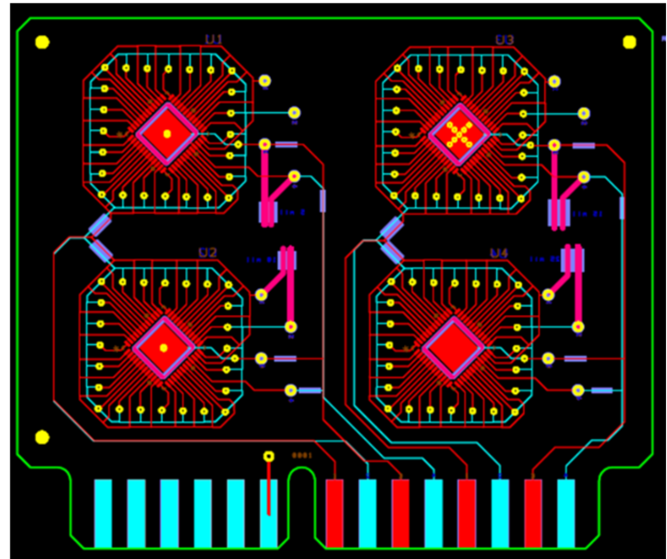

Figure 7: SIR Test Board Design

Figure 8 is a small subset of a data study to evaluate solder paste, reflow conditions, no cleaning and cleaning. The sensor board provides insight into each of these options. An OEM can use this data to determine optimal processing conditions for building their hardware. The ability to do site specific analysis helps the OEM select the right materials, cleaning options and risk profile for specific component types on the finished board. The data subset is from a joint Kester / Kyzen study.

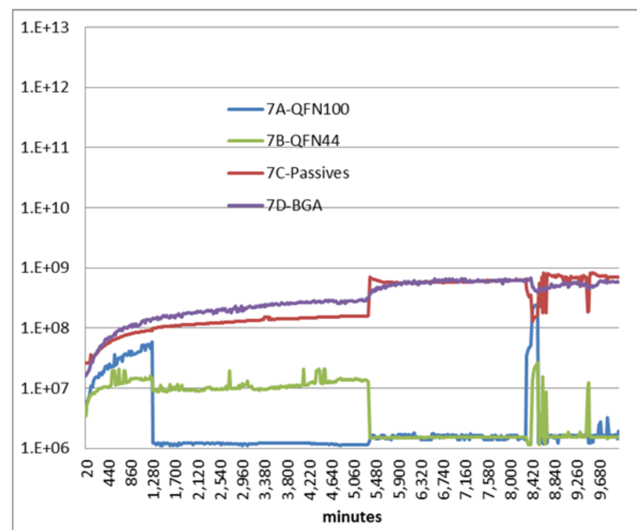

Figure 8a: Ramp to Spike Reflow Profile for a Specific Solder Paste Not Cleaned

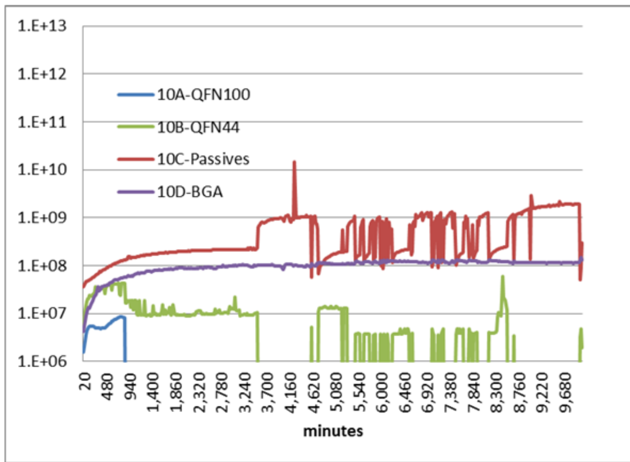

Figure 8b: Soak Reflow Profile for a Specific Solder Paste Not Cleaned

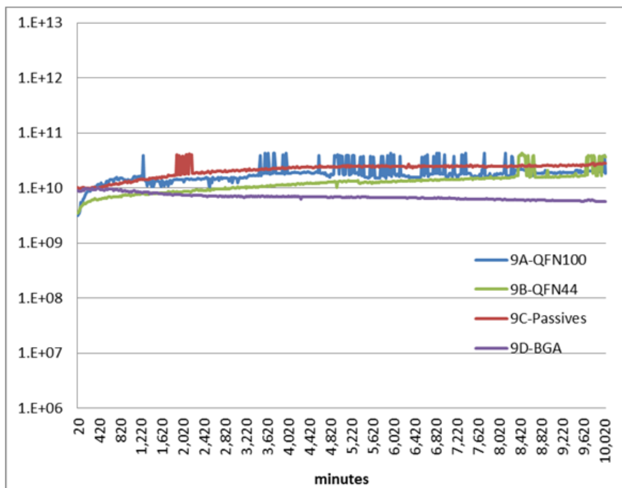

Figure 8c: Ramp to Spike Reflow Profile for a Specific Solder Paste Cleaned

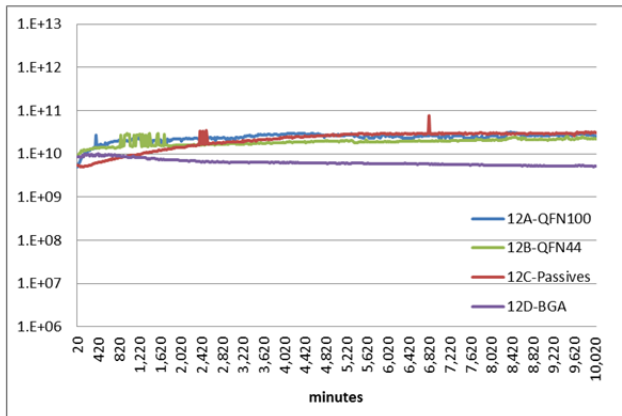

Figure 8d: Soak Reflow Profile for a Specific Solder Paste Cleaned

The data findings from this solder paste show significant differences based on the processing conditions used in the study. The test board design and methodology used provides greater information into determining the process conditions needed to build reliable hardware.

WHY CLEAN A NO-CLEAN FLUX

Flux compositions are a soldering aid designed to facilitate metallurgical bonding. Rosin/Resin structures are oxygen barriers designed to prevent re-oxidation during the soldering process.[7] The flux component is consumed just as the solder is reflowing. The major constituents used to engineer flux are rosin/resin, carrier solvent, activator and rheological additives. The activator in the flux is needed to remove the oxide layer.

When running a no-clean process, rosin/resin is an important ingredient for reliability. After reflow, the rosin/resin forms a protective layer, encapsulates active residues and provides a water impervious coating. Leakage currents and dendrites are more prone to form and propagate with active residues trapped under bottom terminated components. The problem is compounded when the standoff gaps are below 2 mils (Figure 9). When outgassing channels are blocked, flux residue accumulates and starts to underfill and bridge conductors. The residue is typically wet and active. As the distance between conductive paths is reduced, the problem is compounded.

Figure 9: Flux Accumulates Under Bottom Terminations

No-Clean soldering materials are a soldering aid for building reliable PCBs. No-Clean flux development and innovation has captured a dominate market position. The products perform well, improve printing yields and enable soldering of miniaturized components. Under the right conditions no-clean flux residues are safe and not prone to electrochemical migration. No-clean is cost effective, safe and reliable. These beneficial properties are compromised when no-clean flux is not properly outgassed and heat activated.

Many believe that no-clean flux can be used in any manner and still be safe and reliable. Contrary to this myth, no-clean flux when used improperly can lead to electrochemical migration and dendritic growth (Figure 10). Leakage current propagation leads to intermittent failures and with time will eventually short the part. So, what is the proper use of no-clean flux?

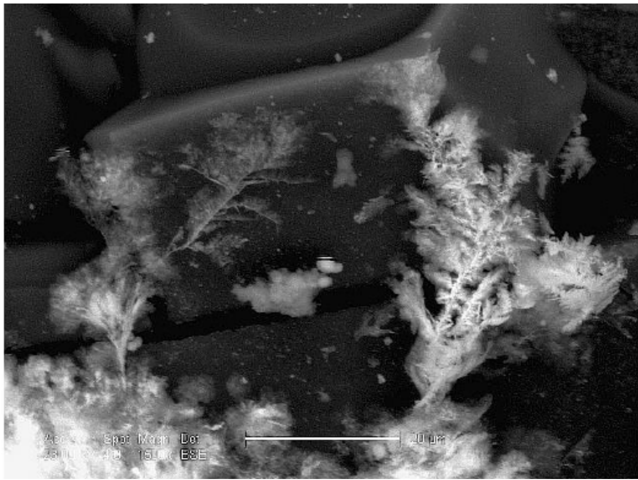

Figure 10: Leakage Growth under BTCs[8]

During pre-heat, flux solvents and moisture outgas. As temperature rises near liquidus, activators remove oxide layers. Flux redox reactions take place. For example, Quad Flat No-Lead components have a large ground lug under the component termination. Low standoff heights in combination with the large ground lug close off outgassing paths. Key problems persist:

1. Flux residue underfills the component
2. Activators may not see the necessary heat to render the residue benign
3. Very challenging to clean
4. In harsh environments, there is a high risk of electrochemical migration

As noted from the data findings in Figures 8a-8d, cleaning reduces risk and improves resistivity levels.

For both cleaning and no-clean processing conditions, increasing the components standoff gaps provides the following benefits:

1. Flux has a channel to outgas
2. Level of flux under the component can be reduced by upwards to 80%
3. Residue under the component termination is benign

There are a number of options for increasing standoff gaps. The problem is that many of these options add cost to the design.

1. Increasing the plating thickness on the bump leads
2. Preform placed onto the ground lug
3. Increase solder paste thickness on bump leads
4. Removal of solder mask under component
5. Solder mask window design
6. Higher copper weights.

CONCLUSION

Reliable hardware is more challenging to build due to component size miniaturization, residues trapped under bottom terminations, shorter distance between conductors, higher pinout devices in a small footprint, increased electrical field and environmental factors. Insufficiently clean under component terminations can cause problems due to intermediate connections, corrosion, electrical shorts and arching. These effects can negatively impact device functionality and end user requirements.

Poor workmanship is costly. On products that must perform as promised, these effects can compromise national security and place people's lives at risk. Even on products that are not critical to national security and human life, uninterrupted service is no longer tolerated by end users. Business is lost when products do not provide long term reliability. Cleaning can improve device reliability by removing residues that can mobilize ionic residues.

To clean under leadless components several process factors must be aligned. The cleaning agent must match up to the soil and cleaning machine. Dissolution of the residue at a fast rate is critical. Equally critical, is the cleaning tool ability to deliver the cleaning agent to the soil. Other factors such as material compatibility, controlling the cleaning agent, temperature, wash time, worker safety and cost must be considered.

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